REMARKS

Claims 1-6 and 11-28 are pending. Claims 23 and 28 have been amended with this response to include the allowable elements of allowed independent claim 1. Reconsideration of the application is respectfully requested based on the following remarks.

I. ALLOWED SUBJECT MATTER

Applicant acknowledges with appreciation the allowance of claims 1-6, 11-18 and 25-27.

II. REJECTION OF CLAIMS 19-24 and 28 UNDER 35 U.S.C. § 103(a)

Claims 19-24 and 28 were rejected under 35 U.S.C. § 103(a), as being unpatentable over U.S. Patent No. 7142671 to Qi et al. (hereinafter Qi) in view of US Patent 5099517 to Gupta (hereinafter Gupta). Withdrawal of the rejection is respectfully requested for at least the following reasons.

i. Neither Qi nor Gupta teach a security processing circuit coupled between the bus interface and the media access control system, the security processing circuit comprising a single DES engine operable to perform 3DES processing, as recited in claim 19.

As the Office action of 6/27/2008 admits at the bottom of Page 2, Qi does not disclose the bus interface and the Media Access Control system (MAC), as Claim 19 recites, however the Office Action further indicates that Gupta discloses in Fig. 3 a Node processor interface (item 64' of Fig. 3) to represent the network interface device and a MAC interface (item 20 of Fig. 3) to represent the MAC of claim 19 and 28.

However, Fig. 3 of Gupta does not provide ***a security processing circuit coupled between the bus interface and the media access control system***, as recited in claim 19. Gupta provides no such single DES engine **coupling between** the

Node processor interface (item 64' of Fig. 3) and MAC interface (item 20 of Fig. 3), as recited in claim 19.

In addition, the Node processor interface (item 64' of Fig. 3) of Gupta, as cited, can not adequately represent the bus interface (*e.g.*, 9 of Fig. 1E) of the present invention, as it is not ***coupled with a host bus in the host system*** (*e.g.*, 7) as recited in claim 19.

Further, Node processor interface (item 64' of Fig. 3) of Gupta, as cited, can not adequately represent the bus interface (*e.g.*, 9 of Fig. 1E) of the present invention, as it is not ***coupled with a host bus in the host system*** (*e.g.*, 7 of Fig. 1E) as recited in claim 19, nor does Gupta recite a network interface device (*e.g.*, 6 of Fig. 1E of the present invention) ***comprising this bus interface*** as recited in claim 19. Also, MAC interface (item 20 of Fig. 3) of Gupta, as cited, can not constitute the MAC system (*e.g.*, 10 of Fig. 1E) of the present invention, as it is not ***coupled between the network interface device*** (*e.g.*, 6 of Fig. 1E) ***and the network*** (*e.g.*, 8 of Fig. 1E) as recited in claim 19, if Node processor interface (item 64' of Fig. 3) of Gupta is used to represent the network interface device (*e.g.*, 6).

Accordingly, not all features of independent claim 19 are disclosed by Qi, or Qi in view of Gupta, and withdrawal of the rejection of claim 19 and claims 20-22 which depend therefrom is respectfully requested.

ii. Neither Qi nor Gupta teach or suggest a method of 3DES processing using a single DES engine having a clock input for timing clock cycles of the first, second and third single DES processing operations, wherein the first, second and third DES processing operations have a duration of two clock cycles each, as recited in claim 23.

Independent claim 23 has been amended to further include the presently allowable elements from independent claim 1, in particular, now further reciting *using* ***a single DES engine having a clock input for timing clock cycles of the first, second and third single DES processing operations, wherein the first, second***

and third DES processing operations have a duration of two clock cycles each, as recited in claim 23. Neither Qi nor Gupta teach or suggest this clock cycle timing and the two clock cycle time duration.

Accordingly, not all features of independent claim 23 and depending claim 25 are disclosed by Qi, or Qi in view of Gupta, and withdrawal of the rejection is respectfully requested.

iii. Neither Qi nor Gupta teach or suggest a security processing circuit comprising a clock input coupled to the single DES engine for timing clock cycles of the first, second and third single DES processing operations, wherein the 3DES security processing is completed in eight clock cycles, as recited in claim 28.

Independent claim 28 has been amended to include all the allowable elements of claim 1 with the exception of the final alternate (or'd) element: *"or wherein the first, second and third DES processing operations have a duration comprising two clock cycles each"*. In particular, claim now includes the allowable element: *"and* ***a clock input coupled to the single DES engine for timing clock cycles of the first, second and third single DES processing operations, wherein the 3DES security processing is completed in eight clock cycles****."* Neither Qi nor Gupta teach or suggest this clock input to the single DES engine and the completion of the 3DES processing in eight clock cycles. Thus claim 28 is not believed to be anticipated by Qi or Qi in view of Gupta, for at least this reason.

Accordingly, not all features of independent claim 28 are disclosed by Qi or Qi in view of Gupta, and favorable acceptance of the claim is respectfully requested.

III. CONCLUSION

For at least the above reasons, the claims currently under consideration are believed to be in condition for allowance.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 50-1733, AMDP783US.

Respectfully submitted,
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